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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,630	07/24/2003	Akiyoshi Tamura	L8462.03106	9060

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EXAMINER

HUYNH, ANDY

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No. 10/625,630	Applicant(s) TAMURA ET AL.	
	Examiner Andy Huynh	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

In the Amendment filed 12/21/2004, claims **1-14** are canceled and new claims **15-28** are added are acknowledged. Accordingly, claims **15-28** are currently pending in the application.

Response to Arguments

Applicant's arguments with respect to claims 15-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims **15-20** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant introduces the new matter by adding:

“a gate electrode extending from the surface of said epitaxial substrate to said buffer layer” into claims **15** and **19**.

The added matter(s) is(are) not supported in the Specification and it (they) (is) are not satisfactory resolved and consequently raise doubt as to possession of the claimed invention at the time of filing.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **21-24 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Inata et al. (USP 4,593,301 hereinafter referred to as "Inata") in view of Nakamura Toshihiro (JP 03-250742 hereinafter referred to as "Nakamura").

Regarding claims **21 and 24**, Inata discloses in Fig. 7 and the corresponding texts as set forth in column 5, line 60-column 7, line 15, a method of manufacturing a heterojunction field effect transistor/a high electron mobility transistor (HEMT), the method comprising:

epitaxially forming a composite substrate, having a plurality of semiconductor layers on a semi-insulative substrate 11, the semiconductor layers including a semiconductor layer that serves as an active layer/a GaAs channel layer 12A and at least one other semiconductor layer, formed over the upper side or both over the upper side and under the lower side of said active layer, that serves as an N-type carrier supply layer/an N-type AlGaAs 15 for supplying an electron to said active layer/the GaAs channel layer;

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forming a gate electrode 20 on said composite substrate; and

forming N-type source and drain areas 17, by carrying out:

ion injection for forming N-type semiconductors in predetermined areas of said composite substrate, each of said source and drain areas formed to one side of said gate electrode, and

an annealing process for activating the ion injected areas.

Inata fails to teach said upper-side N-type carrier supply layer, between said source area and said drain area, is doped with Selenium (Se) or Tellurium (Te), or at least one of said upper- and lower-side N-type carrier supply layers, between said source area and said drain area, is doped with Selenium (Se) or Tellurium (Te). Nakamura teaches in Fig. 1 a semiconductor device comprises an electron/carrier supply layer 5 is doped with Selenium (Se) to obtain a high-speed semiconductor device whose carrier mobility is high and whose carrier concentration distribution inside the substrate face is uniform as set forth in the English Abstract. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form an electron/carrier supply layer doped with Selenium (Se), as taught by Nakamura in order to obtain a high-speed semiconductor device whose carrier mobility is high and whose carrier concentration distribution inside the substrate face is uniform.

Regarding claims **22 and 23**, Inata and Nakamura disclose the all claimed limitations except for the active layer is formed of InGaAs and said upper-side N-type carrier supply layer is formed of InAlAs or at least one of said upper- and lower-side N-type carrier supply layers is formed of InAlAs. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form an InGaAs layer as the active layer and the N-type carrier

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supply layer formed of InAlAs, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 27, Inata discloses the annealing process for activating the ion injected areas is carried out in a manner of lamp annealing (col. 6, lines 12-20).

Claims 25, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inata et al. (USP 4,593,301 hereinafter referred to as "Inata") in view of Shakuda (USP 5,825,052).

Regarding claim 25, Inata discloses in Fig. 7 and the corresponding texts as set forth in column 5, line 60-column 7, line 15, a method of manufacturing a heterojunction field effect transistor/a high electron mobility transistor (HEMT), the method comprising:

epitaxially forming a composite substrate, having a plurality of semiconductor layers on a semi-insulative substrate 11, said plurality of semiconductor layers including a semiconductor layer that serves as an N-type active layer/a GaAs channel layer 12A;

forming a gate electrode 20 on said composite substrate; and

forming N-type source and drain areas 17, by carrying out:

ion injection for forming N-type semiconductors in predetermined areas of said composite substrate, each of said source and drain areas formed to one side of said gate electrode, and

an annealing process for activating the ion injected areas.

Inata fails to teach said semiconductor layer serving as said N-type active layer is doped with Selenium (Se) or Tellurium (Te). Shakuda teaches in Fig. 1 a semiconductor light emitting device comprises an active layer 5 is doped with Selenium (Se) or Tellurium (Te) to control the wavelength of emitted light (col. 4, lines 26-30). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form an active layer doped with Selenium (Se) or Tellurium (Te), as taught by Shakuda in order to control the wavelength of emitted light.

Regarding claim 26, Inata and Shakuda disclose the all claimed limitations except for said N-type active layer is an InGaAs layer, a GaAs layer, or an InP layer. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the N-type active layer being an InGaAs layer, a GaAs layer, or an InP layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 28, Inata discloses the annealing process for activating the ion injected areas is carried out in a manner of lamp annealing (col. 6, lines 12-20).

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

02/14/05



Andy Huynh

Patent Examiner